**1.0 AIM:**

Design and analysis inverter using cadence.

1. **SCOPE:**

To study the performance of an inverter.

1. **FACILITIES:**  Cadence Tool

1. **THEORY:**

The inverter is basic gain stage for CMOS circuits typically, the inverter uses common source configuration with either an active resistor for a load or a current sink/source as a load resistor. There are various types of inverter, active pMOS load inverter, current source load inverter, and push pull inverter.The large signal voltage transfer function plot for the push pull inverter can be found in similar manner as a plot for the current source inverter. In comparing a large signal voltage transfer function characteristics between the current source and push pull inverter, It is seen that the push pull inverter has a higher gain assuming identical transistor. This is due the fact that both transistors are being driven by input voltage. Another advantage of push pull inverter is the output swing is capable of operation from rail to rail (VDD to GROUND) The small signal performance of a push pull inverter depends on its operating region. If we assume that both transistor M1 and M2 are in the saturation region, then we will achieve largest voltage gain.

The small signal voltage gain is ,

Vout / Vin = - (gm1+gm2) / (gds1+gds2)

The regions of operations for the push pull inverter are shown on the voltage transfer curve of the figure. This regions are easily found using the definition of Vds(sat) given for the MOSFET. M1 is the saturation region when

VDS1 ≥ VGS1-VTN 🡪 VOUT ≥VIN - 0.7 V

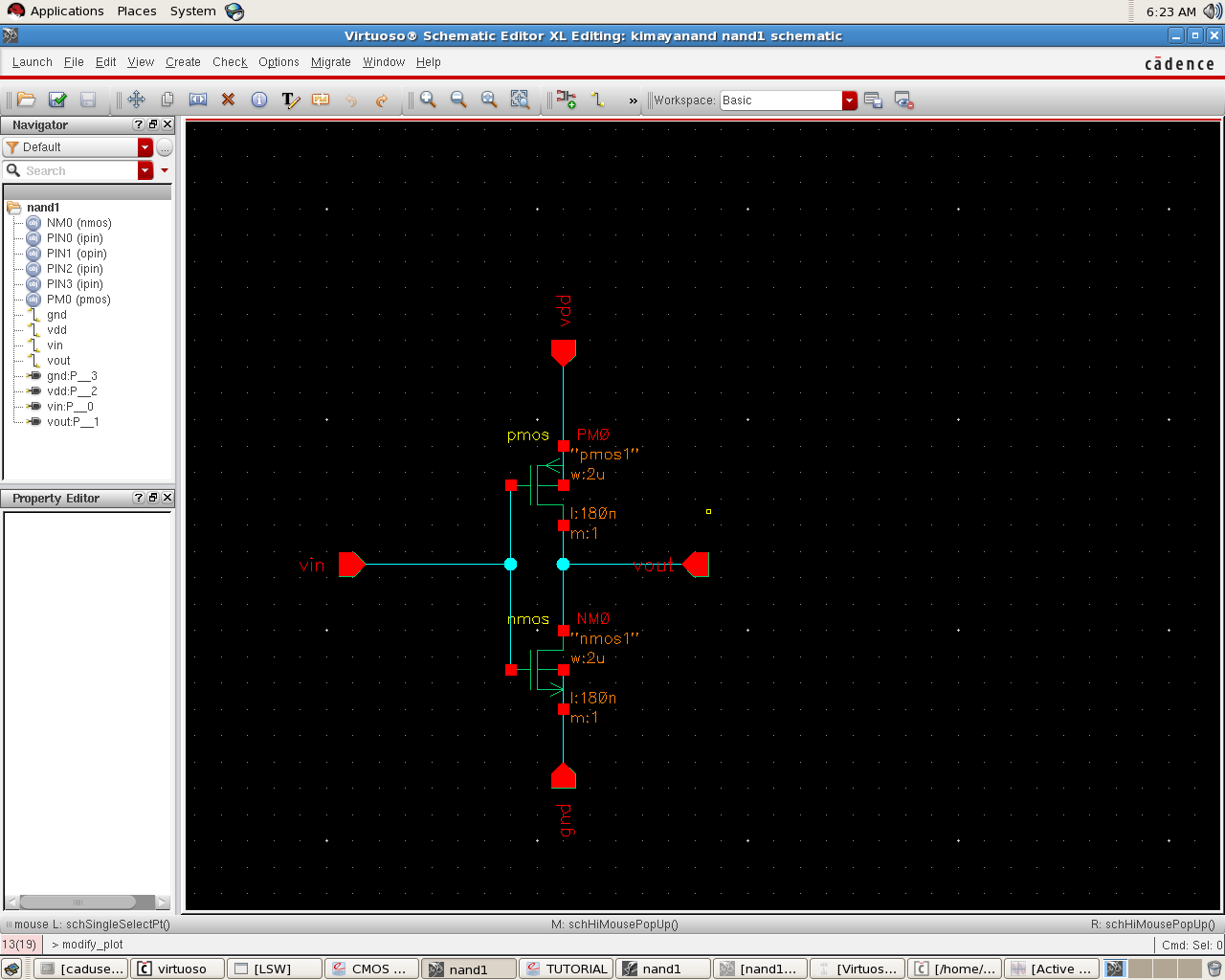
M2 is the saturation region when

VSD2 ≥ VSG2 − VTP 🡪VDD – VOUT ≥ VDD – VGG2 – VTP 🡪 VOUT ≤ 3.2 V

We note the same dependence of the gain on the DC current that was observed for the current source/sink inverters. If Id is 1 µA and W1/L1 = W2/L2 = 1 , then using the parameters , the maximum small signal voltage gain is -276. The output resistance and the -3db frequency response of the push-pull inverter are identical to those of the current source inverter.

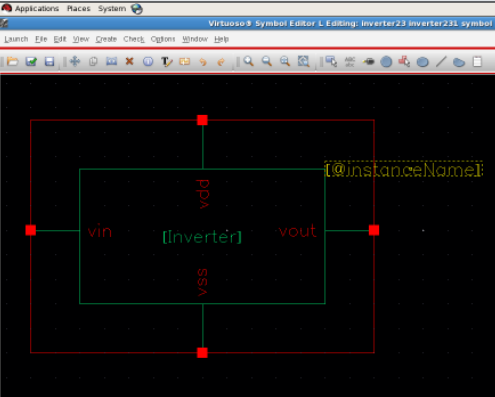
**Design Steps:**

1. Decide suitable cadence environment.
2. Create the proper library and its cell with gpdk180 technology file.
3. Design devices schematic for proper operation.

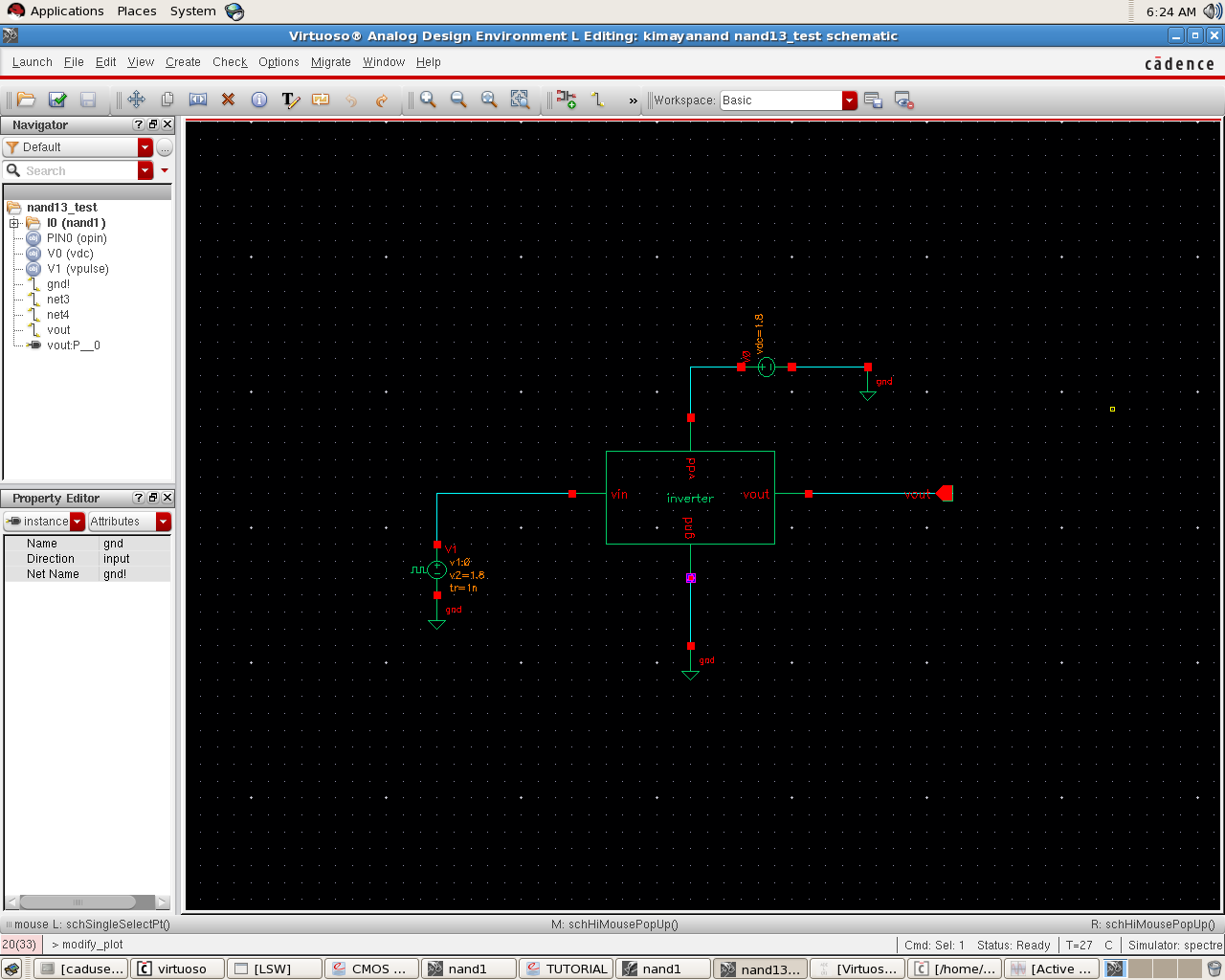
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**Schematic of Inverter**

1. After checking schematic go for symbol creation and design with symbol



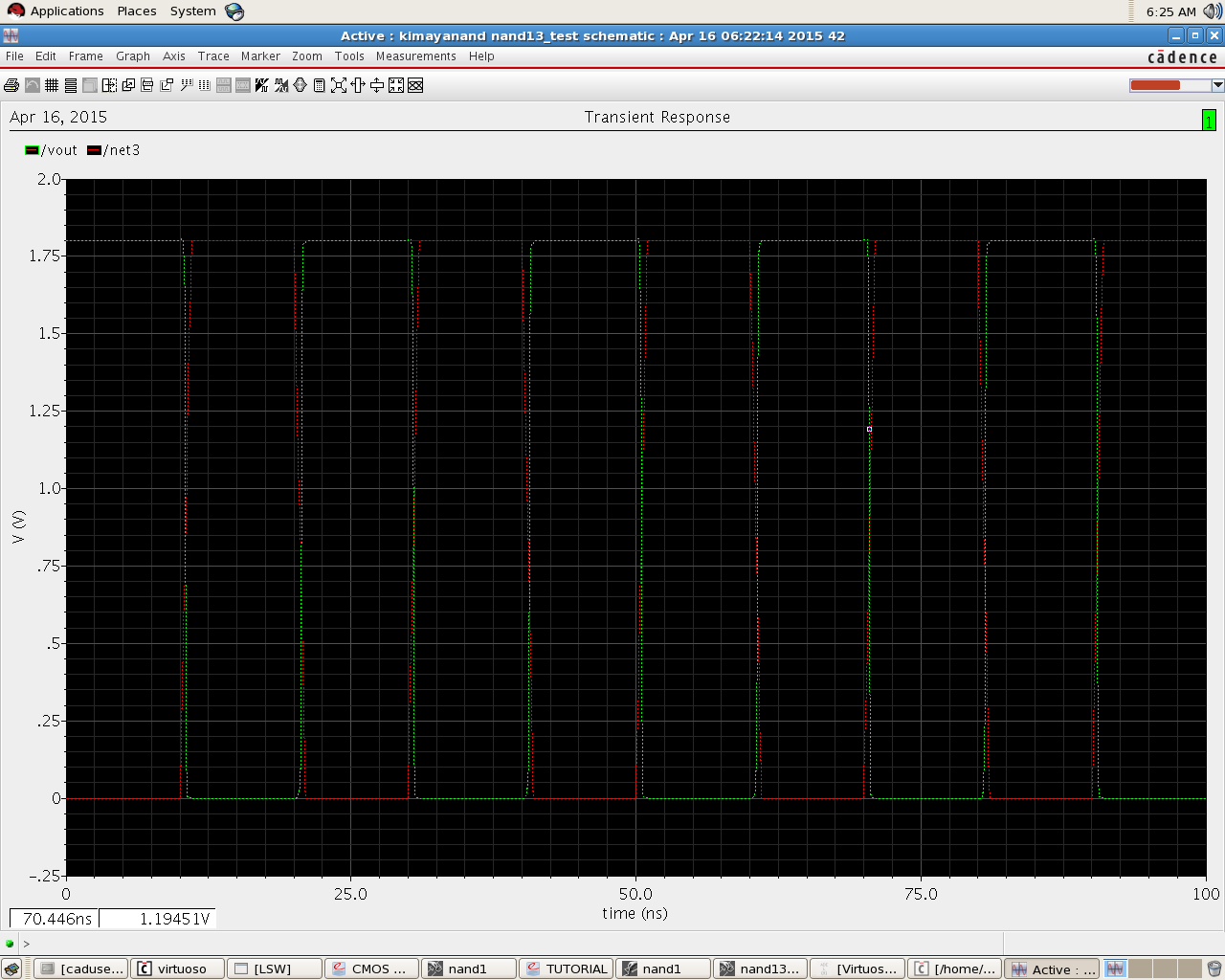
**Symbol of Inverter**



**Test circuit of Inverter**

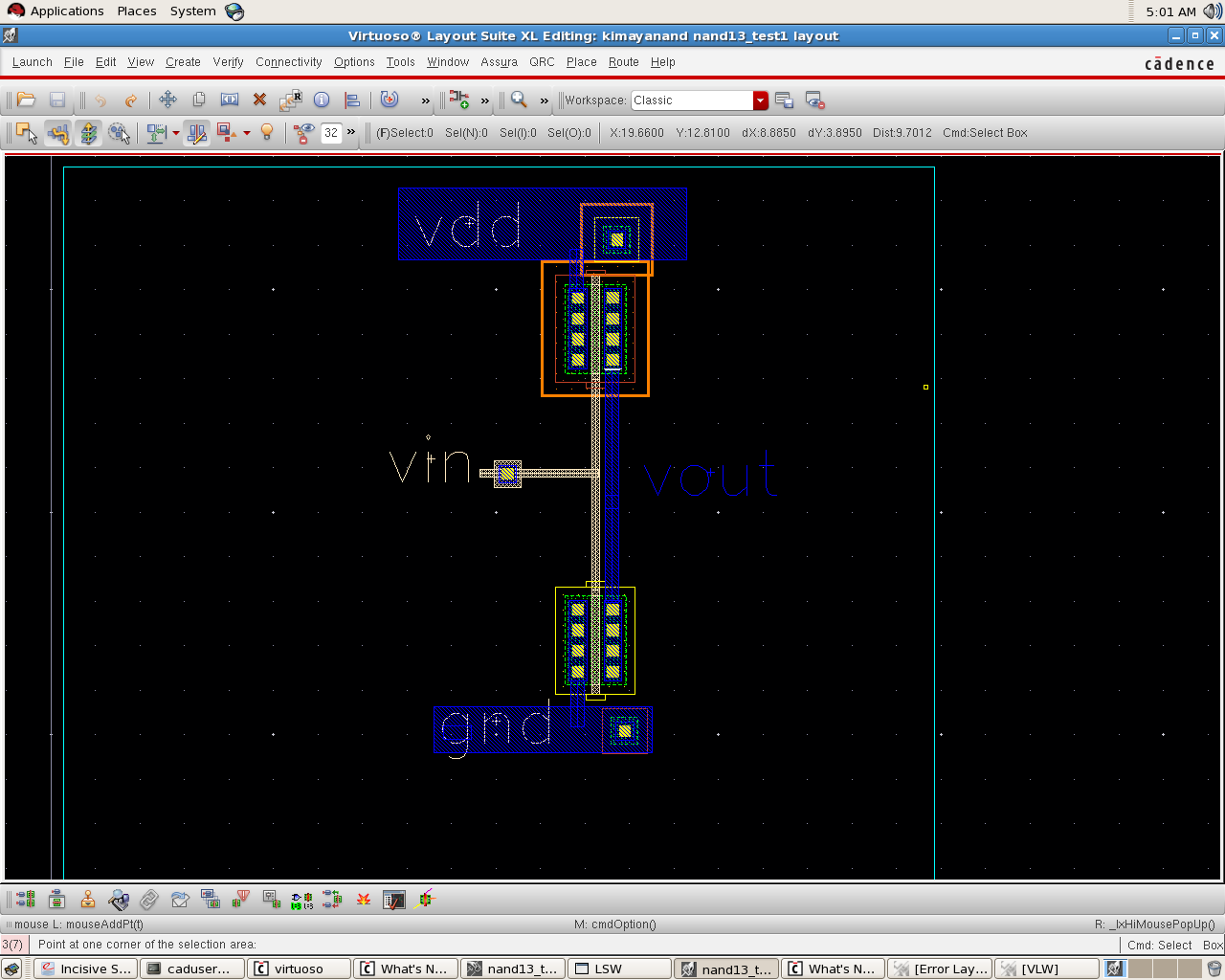
**5.0 RESULT**

Check for the design operation.



**Output waveform of Inverter**

**LAYOUT:**

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**Layout of Inverter**

**6.0 CONCLUSION**

There are very less numbers of capacitors and resistors and hence design is feasible. However, these values can be reduce by adjusting the position of components and reducing path length.

**7.0 PRECAUTIONS**

Give the specifications correctly and the current through N-MOS and P-MOS must be equal.